

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit: To Be Assigned

Examiner: To Be Assigned

In Re PATENT APPLICATION Of:

Applicant : Toshio TERAISHI)

Appln. Ser. No. : To Be Assigned)

Filed : July 14, 2003)

For: ANALOG VOLTAGE OUTPUT DRIVER)
LSI CHIP HAVING TEST CIRCUIT)

Attorney Ref. : 03DCOAI030)

**INFORMATION
DISCLOSURE
STATEMENT**

July 14, 2003

Commissioner for Patents
Alexandria, VA 22313-1450

Sir:

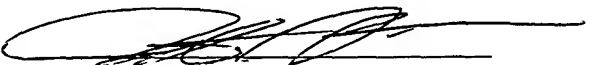
This is an Information Disclosure Statement submitted in compliance with the timing requirements of 37 C.F.R. § 1.97(b)(1).

Attached is a copy of one Japanese laid-open patent document. The document is listed on the attached Form PTO-1449. Moreover, English language abstract of the document is also attached.

Since this Information Disclosure Statement is being filed with the application, no certification or fee is required, and the requirements of 37 C.F.R. §§ 1.97 and 1.98 are deemed to be fully met as to all documents submitted. Consideration of the submitted documents is respectfully requested.

Respectfully submitted,

July 14, 2003
Date


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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT				Atty Docket 03DCOAI030		U.S. Application No.: To Be Assigned			
				Applicant Toshio TERAISHI					
				U.S. Filing Date: July 14, 2003		Group To Be Assigned			
U.S. PATENT DOCUMENTS									
Examiner Initial		Document Number	Date	Name	Class	Sub-Class	Filing Date		
	AA								
	AB								
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FOREIGN PATENT DOCUMENTS									
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	AL	P2000-131393A	5/12/00	Japan	G01R	31/28	Abstract		
	AM								
	AN								
	AO								
OTHER (Including Author, Title, Date, Pertinent Pages, etc.)									
	AR								
	AS								
Examiner					Date Considered				
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.									